Chapter 1:
Digital Design Concepts
Part 1
As you already know..
Most natural quantities that we see are **analog** and vary continuously. Analog systems can generally handle higher power than digital systems.

Digital systems can process, store, and transmit data more efficiently but can only assign discrete values to each point.
Many systems use a mix of analog and digital electronics to take advantage of each technology. A typical CD player accepts digital data from the CD drive and converts it to an analog signal for amplification.
Digital electronics uses circuits that have two states, which are represented by two different voltage levels called HIGH and LOW. The voltages represent numbers in the binary system.

Binary Digits and Logic Levels

In binary, a single number is called a *bit* (for *binary digit*). A bit can have the value of either a 0 or a 1, depending on if the voltage is HIGH or LOW.
Example: for a 3.3 V CMOS technology

High: 2 to 3.3 V
Low: 0 to 0.8 V

Identify the level:
• 0.5 V
• 2.5 V

Unacceptable: 0.8 to 2 V
Low: 0 to 0.8 V
Digital waveforms change between the LOW and HIGH levels. A positive going pulse is one that goes from a normally LOW logic level to a HIGH level and then back again. Digital waveforms are made up of a series of pulses.

(a) Positive–going pulse

(b) Negative–going pulse
Actual pulses are not ideal but are described by the rise time, fall time, amplitude, and other characteristics.
Delay Definitions

\[ V_{in} \]

\[ V_{out} \]

- \( t_{PHL} \)
- \( t_{PLH} \)
- \( t_f \)
- \( t_r \)

50% 10% 90%

\( t \)
Propagation Delay

**Definition 1**

- \((t_{PHL} + t_{PLH})/2\)

**Definition 2**

- Max \((t_{PHL}, t_{PLH})\)
Periodic pulse waveforms are composed of pulses that repeats in a fixed interval called the **period**. The **frequency** is the rate it repeats and is measured in hertz.

The **clock** is a basic timing signal that is an example of a periodic wave.

What is the period of a repetitive wave if \( f = 3.2 \text{ GHz} \)?

\[
T = \frac{1}{f} = \frac{1}{3.2 \text{ GHz}} = 313 \text{ ps}
\]
Pulse Definitions

In addition to frequency and period, repetitive pulse waveforms are described by the amplitude \(A\), pulse width \(t_w\) and duty cycle. Duty cycle is the ratio of \(t_w\) to \(T\).
A timing diagram is used to show the relationship between two or more digital waveforms,

A diagram like this can be observed directly on a logic analyzer.
Data can be transmitted by either serial transfer or parallel transfer.
Basic Logic Functions

AND
True only if *all* input conditions are true.

OR
True only if *one or more* input conditions are true.

NOT
Indicates the *opposite* condition.
And, or, and not elements can be combined to form various logic functions. A few examples are:

The comparison function

Basic arithmetic functions
Basic System Functions

The encoding function

The decoding function
The data selection function

- **Basic System Functions**

- **Multiplexer**
  - Switching sequence control input
  - Data from A to D
  - Data from B to E
  - Data from C to F
  - Data from A to D

- **Demultiplexer**
  - Switching sequence control input
  - Data from D to A
  - Data from E to B
  - Data from F to C

The diagram illustrates the switching sequence and control input for both the multiplexer and demultiplexer.
Basic System Functions

The counting function

Counters...

...and other functions such as code conversion and storage.
One type of storage function is the shift register, that moves and stores data each time it is clocked.

Initially, the register contains only invalid data or all zeros as shown here.

First bit (1) is shifted serially into the register.

Second bit (0) is shifted serially into register and first bit is shifted right.

Third bit (1) is shifted into register and the first and second bits are shifted right.

Fourth bit (0) is shifted into register and the first, second, and third bits are shifted right. The register now stores all four bits and is full.
**Clock**

A basic timing signal in a digital system; a periodic waveform used to synchronize actions.
1. The time measurement between the 50% point on the leading edge of a pulse to the 50% point on the trailing edge of the pulse is called the

   a. rise time
   b. fall time
   c. period
   d. pulse width
2. The time measurement between the 90% point on the trailing edge of a pulse to the 10% point on the trailing edge of the pulse is called the

   a. rise time
   b. fall time
   c. period
   d. pulse width
3. The reciprocal of the frequency of a clock signal is the
   a. rise time
   b. fall time
   c. period
   d. pulse width
4. If the period of a clock signal is 500 ps, the frequency is

a. 20 MHz

b. 200 MHz

c. 2 GHz

d. 20 GHz
5. A shift register is an example of a
   a. storage device
   b. comparator
   c. data selector
   d. counter
6. A device that is used to switch one of several input lines to a single output line is called a

   a. comparator
   b. decoder
   c. counter
   d. multiplexer
Figure 1.1. A silicon wafer (courtesy of Altera Corp.).
Cutaway view of DIP (Dual-In-line Pins) chip:

• TTL chips (7400 series)
• CMOS chips (4000 series)

SN 74 ALS 00 N

SN : Manufacturer (Texas Instruments)
74: 74-series
ALS: Logic Family (Advanced Low Power)
00: Logic Function (Quad 2-input NAND)
N: Package (Plastic DIP)
Integrated Circuits

DIP chips and surface mount chips

Pin 1

Dual in-line package

Small outline IC (SOIC)
Integrated Circuits

Other surface mount packages:

- SOIC
- PLCC
- LCCC
A typical ball-grid array (BGA) package configuration.
Digital Hardware

- Standard Chips
- Programmable Logic Devices
- Custom Designed Chips
Figure 1.6. A printed circuit board.
A digital hardware system
Fixed-function logic
(Standard Chips)

A category of digital integrated circuits having functions that cannot be altered.
Figure 3–61  Pin configuration diagrams for some common fixed-function IC gate configurations.
Programmable logic

A category of digital integrated circuits capable of being programmed to perform specified functions.
Programmable logic devices (PLDs) are an alternative to fixed function devices. The logic can be programmed for a specific purpose. In general, they cost less and use less board space than fixed function devices.

A PAL device is a form of PLD that uses a combination of a programmable AND array and a fixed OR array:
Figure 1.2. A field-programmable gate array chip (courtesy of Altera Corp.).
The basic design loop
Programmable logic.

Programmable logic

- PLDs
  - SPLDs
    - Simple PLDs
  - CPLDs
    - Complex PLDs
- FPGAs
  - Field Programmable Gate Arrays
- PROM, Programmable ROMs
Block diagrams of simple programmable logic devices (SPLDs).
General block diagram of a CPLD.
Basic structure of an FPGA.
Basic configuration for programming a PLD or FPGA.
Programmable Logic Softwares

- Altera’s QuartusII
- Xilinx ISE
- Lattice
Basic PLD design flow

**Design Entry**
- Schematic
- Source Codes (HDL, hardware description language)

**Functional Simulation**
- Verify that the circuit functions as expected

**Synthesis**
- Converts schematic or HDL codes into logic gates circuit

**Timing Simulation**
- Considers propagation delay of the circuit

Program the PLD chip
Custom Designed Chips

- The circuit is designed to be optimized, therefore better performance.
  - Less chip area, higher speed, lower power, etc.
- Consists of bigger circuits, i.e. can replace multiple standard chips.
- Examples: microprocessor or any chips for a special purpose.