TECHNIQUES IN INTEGRATED CIRCUIT (IC) FAILURE ANALYSIS

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Failure analysis (FA) plays an important role in the development and manufacturing of integrated circuits. It provides necessary information for technology advancement and for corrective action to improve quality and reliability. In this paper the commonly used techniques in integrated circuits failure analysis are discussed. The paper also describes the basic FA flow consists of fault localization, deprocessing, defect localisation and inspection characterisation.

INTRODUCTION

The failure of electronic or mechanical components is best described by the bath-tub curve [1] as shown in Fig. 1. For semiconductor devices, the infant mortality portion of the curve are failures due to defects during fabrication, improper design of the component, or random failures that have not failed during fabrication screening processes. The normal operation of the devices is described by the useful life portion of the curve. Stresses due to high temperature, high voltage current, humidity, vibration, mechanical or thermal shock are examples of failures during this period. The final curve represents the wear out failures. Examples of these types of failures are corrosion, electrical leakage, insulation breakdown, cracking of encapsulation due to the deterioration of the material, and cracks in the bond wires.

Figure. 1: The bath-tub curve – failure types over time

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The objective of failure analysis (FA) is to identify the cause of failure and initiate corrective action. There have been significant improvements and developments in both the techniques and equipment used in the FA works on semiconductor devices [2]. Earlier FA works on semiconductor devices mostly consist of destructive physical analysis using metallographic techniques and optical microscopy. But now due to the microelectronics technology which has rapidly evolved to smaller feature sizes and larger levels of integration, the FA works has progressed to a level of sophistication and complexity matching the components that are to be analysed [2, 3].

In this paper, commonly used FA techniques for integrated circuits are described. The basic FA flow is discussed with emphasis on the application of the microscopy techniques. Some case studies based on the works of other researchers are also described.

CAUSES OF FAILURE

In an IC, the failure is caused by the change of resistance in any electrical path or between any electrical nodes in the device. However, components do not usually fail for electrical reason but are caused by either physical, chemical, or mechanical mechanisms [4]. Approximately 60% of the failures are due to the electrical overstress (EOS) and electrostatic static discharge damage (ESD). Mechanical and chemical effects such as high cycle fatigue or corrosion, will short the circuit by breaking an electrical path contribute approximately 30% of the failures. The remaining 10% of the failures are due to component wear out.

It is necessary to combine a series of electrical and physical steps to localise and identify the ultimate cause of failure. Fig. 2 shows a simplified version of the sequence in a typical FA work [5, 6]. A typical analysis could include many loops between the steps shown as there is a variety nature of components, failures, and detect mechanisms involved.

**Figure 2:** The basic failure analysis flow

FAULT LOCALISATION

Fault localization can be done using both hardware and software diagnostics tools. The size of and complexity of electronic devices make it crucial to accurately localise faults prior to any destructive FA tests. Photon emission microscopy (PEM), liquid crystal hot spot analysis and fluorescent microthermal imaging are examples of hardware diagnostic tools that are used to localise faults [7]. These tools are expensive and require experienced personnel trained in IC architecture, testing and the technique itself in order to optimize the testing processes. Software diagnostic tools rely on the combination of fault simulation and IC design data to determine the fault locations. With suitable software diagnostics, inspection of the identified circuits can begin immediately once a fault list is produced. There are other tools available for fault localisation and Benstetter et al ‘2002 [8] is referred for further reading.

The level of difficulty for fault localization has increased throughout the years. Fig. 3 shows the trend [5, 9] in the projected increase in device complexity versus the projected decrease in minimum defect size. Here the complexity is defined as the sum of the number of transistors and the total wiring length on the IC.
DEPROCESSING

Deprocessing or also known as decapsulation is an FA technique for revealing the internal structure of a device or IC for examination. This is done either by mechanical or chemical methods depending on the package materials [10]. For an example, plastic encapsulation is etched out through a jet delivery system utilising hot fuming nitric acid or sulfuric acid. Depending on the accuracy of fault localization and the nature of the failure, it is sometimes necessary to inspect and remove several layers of insulating films or metal wiring until the fault can be isolated for defect identification and characterisation.

Fig. 4 shows the plan view of an IC after its package has been decapsulated. The image is captured under high powered light microscope.

Figure 3: The Projected increase in relative complexity versus minimum defect size.

Figure 4: IC Package after Chemical decapsulation. Note the missing wire contacts on the bond pads.

DEFECT LOCALISATION AND CHARACTERISATION

Once the fault has been localised to a circuit block or a memory cell, a second localisation step or characterisation process of the fault is usually necessary to further pinpoint the location of
the defect. At this stage it is step by step procedure using the non-destructive techniques to gather as much information as possible about the defect and its location before proceeding to the destructive methods of analysis. Here, apart from the hardware diagnostic tools utilising light or heat mentioned earlier, techniques like internal electrical circuit microprobing to measure signals on conductors of interest and scanning probe microscope to measure the effects of the defect on electrostatic force, atomic force, or capacitance can also be carried out.

INSPECTION AND DEFECT CHARACTERISATION

The final step is to physically detect the defect. This is done after all the necessary steps to localise and characterise the fault have been performed. The defect will also need to be characterised so that enough materials properties of the defect are known to determine the root cause of the defect. There are presently many techniques available to do the characterisation and Soden J. M. & Anderson R. E. ‘1993 [7] is referred for more information. Some of the common techniques are discussed as follows.

Optical Techniques

The simplest way to inspect the failure site is through optical techniques. Optical microscopes [7] allow inspection of failure site under different types of illumination namely bright field, dark field and Nomarski interference contrast. Using high powered optical microscopes of which magnification up to 2000x can be achieved, anomalies for example on relatively long metal wire contacts and circuit blocks can be observed. Infrared (IR) microscopy is another important optical technique. The technique capitalise on the transparency of some semiconductor materials to infrared light to allow the imaging of structures beneath the surface of the material [11]. Irregularity such as large change in doping, the present of a defect and misalignment between layers can be imaged. The only drawback is the lack of spatial resolution which limits the usefulness of IR microscopy in sub-micron devices.

Cross Sectioning

Cross sectioning allows the viewing of a ‘slice’ of an IC. Typically, the process involved mechanical grinding in the direction which is perpendicular to the surface in order to expose the feature of interest. In addition, focus ion beam (FIB) milling [12] can be performed to further localise the area of interest. Following cross sectioning, the sample may be slightly etched to highlight features of interest for observation under various types of microscopes. Fig. 5 shows an optical micrograph of a solder joint between the die and the lead frame of an IC package after cross-sectioning process was done.

Electron Microscope

The scanning electron microscope (SEM) [12] is the mainstay tool in IC FA. Apart from the typical high resolution imaging and elemental analysis, SEM can also image electrical activity of the IC. Care must be taken to minimize the undesirable side effects of the electron beam, such as the shifting of the threshold voltage of MOS transistors.

Secondary electron imaging can locate defects that too small or difficult to image with optical microscopy. Backscattered electron imaging detects differences in atomic number on and below the surface. It’s primarily used to detect sharp atomic number gradients, such as barrier metals, impurities, and metal voids, under the passivation.

Defect such as missing wire as shown in Fig. 6 can be clearly observed by SEM. Further chemical analysis can be performed to determine to elemental composition on the sample.
SEM can be used to image the electrical activity through the voltage contrast (VC) technique [7]. The technique has an important role in failure analysis and reliability improvement since it provides a nondestructive method for observing internal IC operation and the electrical effects of defects. The VC technique creates an image in which the intensity is largely determined by the static voltages on an IC. By analyzing the variations in brightness, the logic levels of a digital IC can be determined and the voltage on internal test nodes can be measured. VC imaging takes advantage of differing secondary electron (SE) emission efficiencies with applied bias on an IC.

The transmission electron microscope [12, 13] is the only method that allows the images with resolution at the atomic scale to be taken and the same time facilitate the process of chemical analysis. However, TEM observation requires very thin samples with electron transparency requirement and this is not only difficult and delicate to prepare but is also time consuming. Here, again FIB milling together with mechanical grinding or polishing process can be used to prepare the samples and facilitate the precise location of the area of interest.

SUMMARY AND CONCLUSION

A basic and systematic approach to FA has been discussed. The technical challenges fall primarily into two categories namely failure site isolation and physical techniques. The failure site isolation challenges are driven primarily by the device complexity and reduced accessibility of the circuits. These will present problems for FA work and require new types of tools and techniques to probe into the IC.
REFERENCES


